35ton FEMB Testing Lessons Learned

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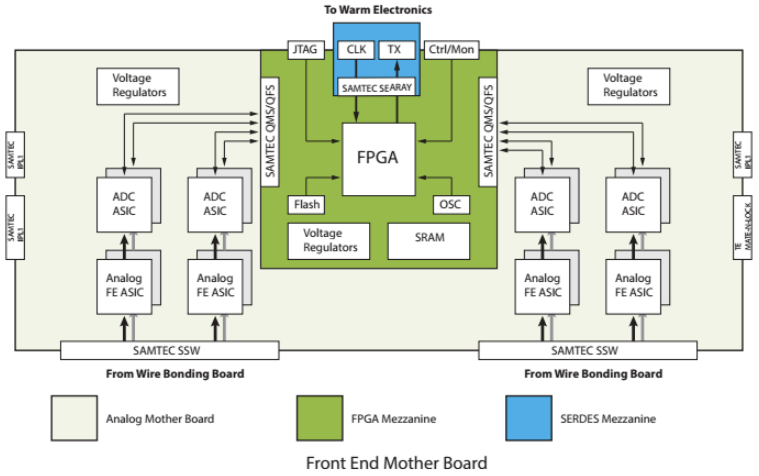
35ton Review
June 2, 2016

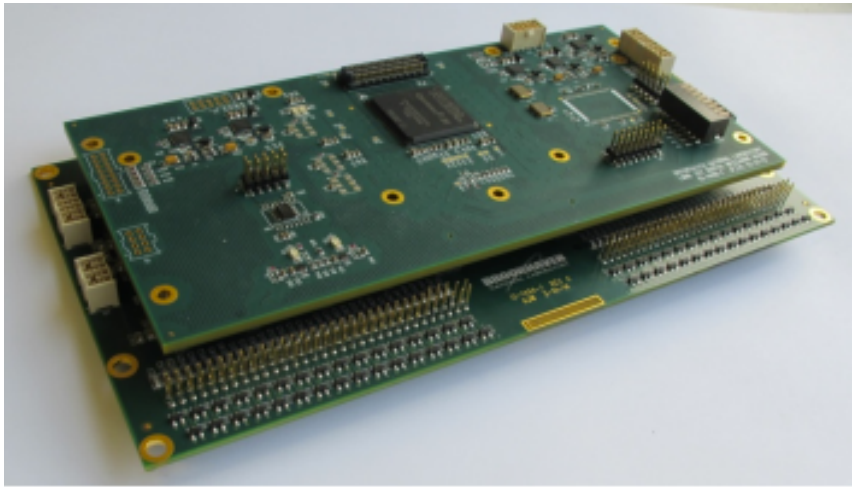
Outline

- Cold front-end motherboard (FEMB)
- People and timeline
- FEMB teststand and testing procedure
- Documentation
- Lessons learned

35ton FEMB



Front End Mother Board



- Analog motherboard
  - 8 16-channel front-end (FE) ASICs
    - Gain and signal shaping
    - MicroBooNE FE ASICs (had been already tested for uBooNE)
  - 8 16-channel ADC ASICs
    - 12-bit ADC at 2 MS/sec
    - V5 ADC ASICs (prototypes)
- FPGA mezzanine
  - Distribute clock/control/ configuration to ASICs
  - Control can be either bi-directional I2C or PGP (to RCEs)
  - Transmit 1.2 Gbps data to warm electronics (x4 links)
  - Distribute internal calibration pulse to FE ASICs
- SERDES mezzanine (not shown)
  - SMA connectors to cold cable

Personnel

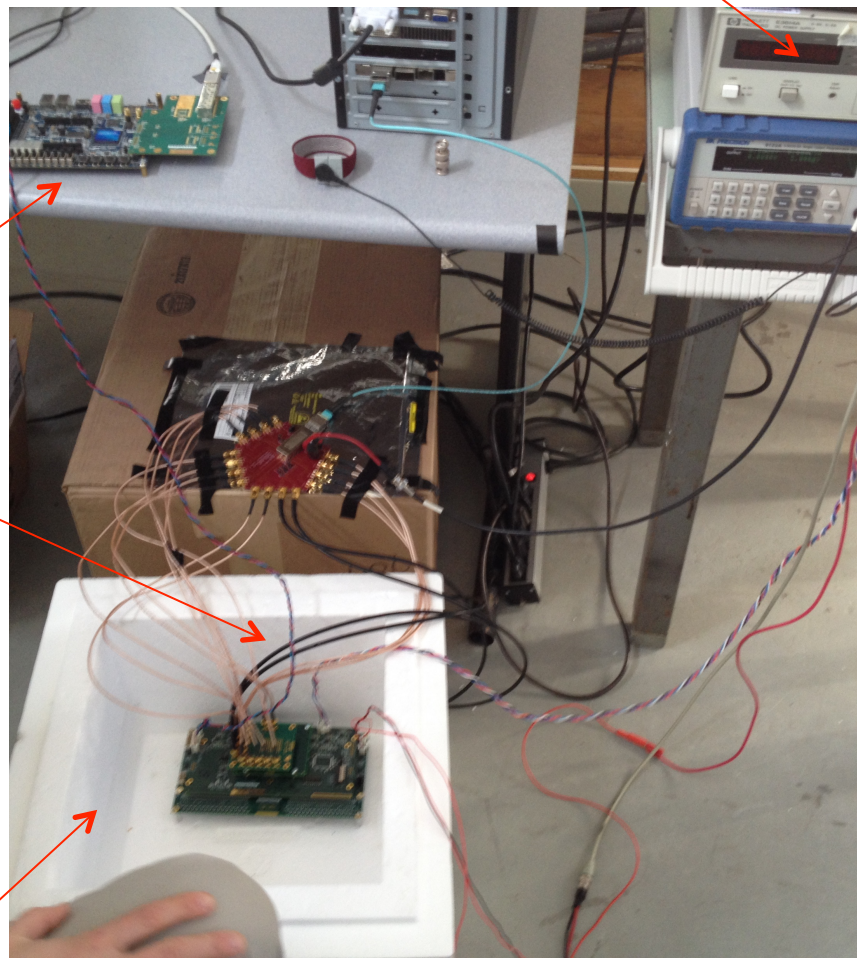
- BNL
  - Brian Kirby (post-doc)
  - Matt Worcester (50% time)
  - Support from BNL Instrumentation team: Hucheng Chen, Jack Fried, Veljko Radeka, Gianluigi DeGeronimo, Neena Nambiar, Emerson Vernon
    - Instrumentation heavily invested in MicroBooNE during testing, many other committments
- Stony Brook
  - Gabriel Santucci and Jay Hyun Jo (grad students)

2015 Timeline

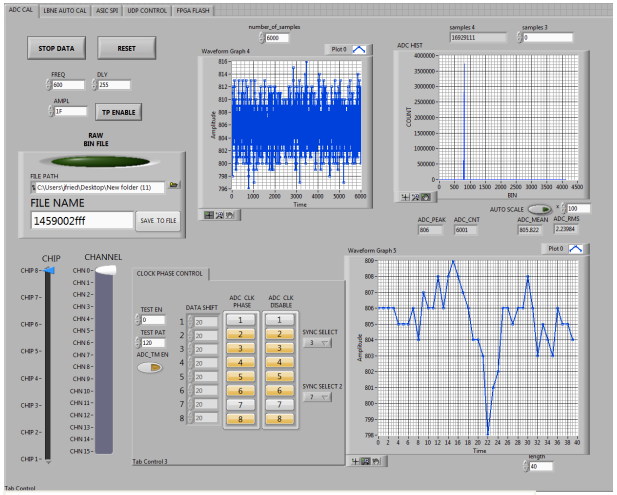
- January
  - Preliminary tests at room temperature with first assembled FEMBs at BNL Instrumentation
  - Develop LN2 testing plan
- February
  - Teststand setup in BNL Physics high-bay
  - First LN2 testing with "production" FEMBs
    - Note that "production" FEMBs for 35ton are actually early prototypes
- April
  - First lot of 4 FEMB sent to Fermilab
- May
  - Second lot of 8 FEMB sent to Fermilab (replacing 2 of the first lot)
  - Work to debug and validate final few FEMB (mostly replacing ASICs that failed in LN2)
- July
  - Final 6 FEMBs sent to Fermilab (no spares)
- August
  - Emergency replacement of one FEMB damaged during installation

FEMB Teststand

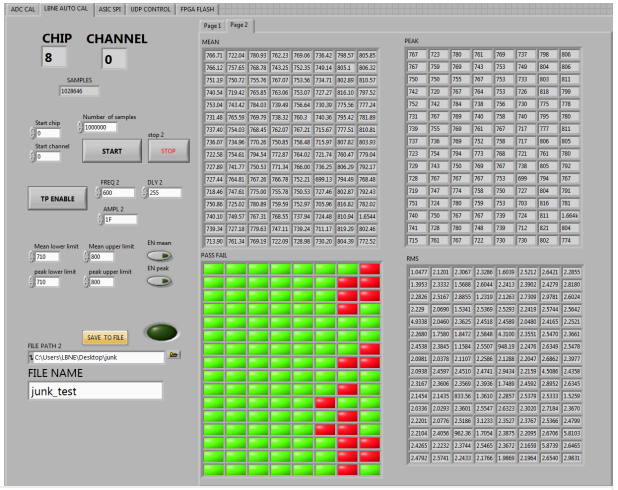
- I2C control done via the "compact DAQ" from BNL
  - Laptop running a LabView GUI using UDP over gig-E to communicate with an Altera Cyclone IV eval board
  - Two SMA cables for the bi-directional data and control connected from eval board to SERDES mezzanine
- This interface was the primary testing tool
  - Used to diagnose problems on FEMB in real-time and save data for later analysis



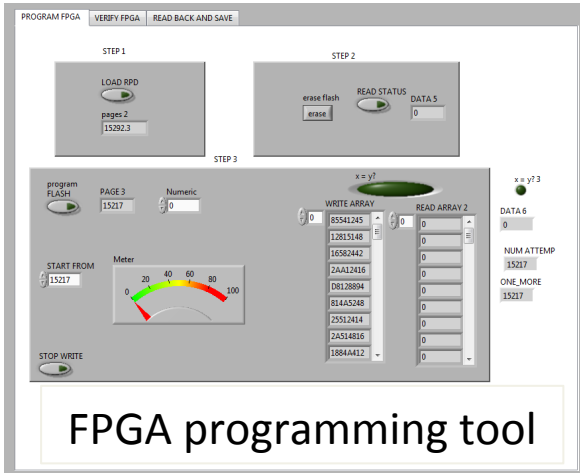
“Compact DAQ” Tools



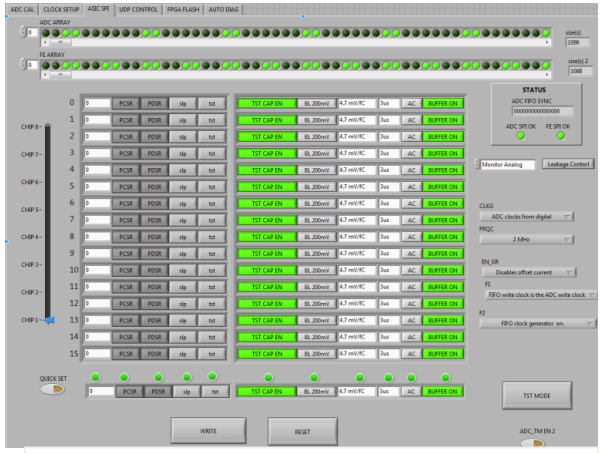
Real-time channel data



Automated debugging tool



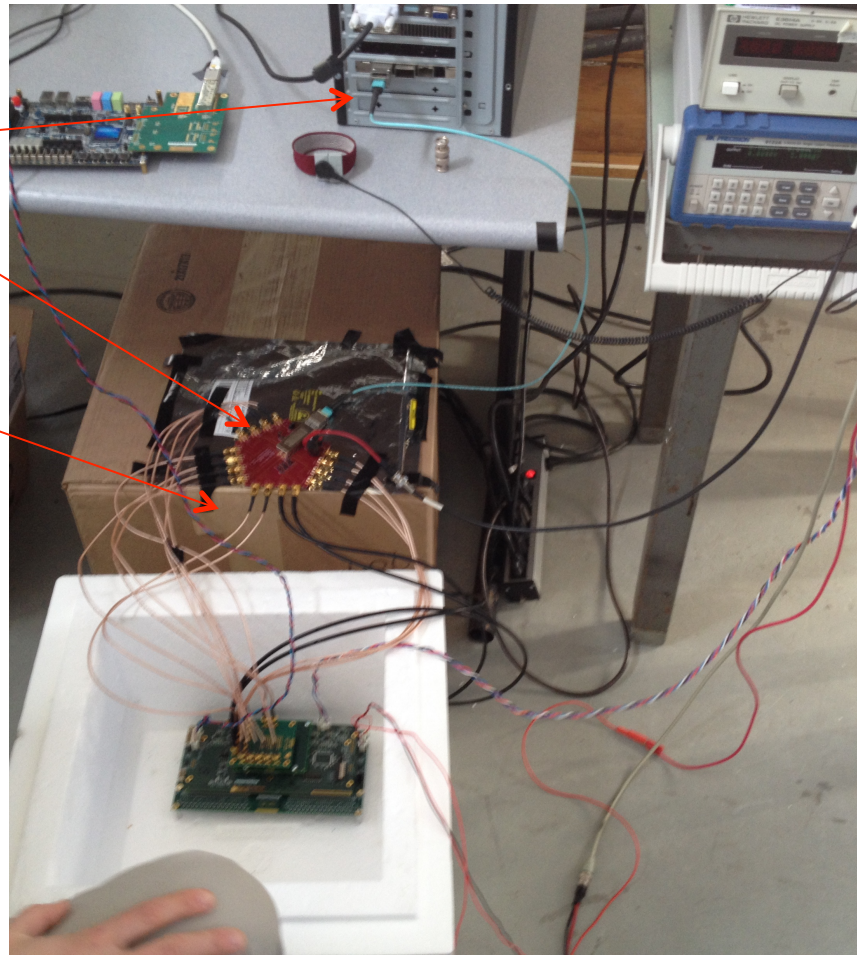
FPGA programming tool



ASIC SPI Programming

FEMB Teststand

- PGP control was done on a Linux desktop PC (RCE interface)
  - Optical fiber from SLAC PGP PCI card to transceiver breakout board (our "warm flange")
  - 16 SMA cables from flange for 4 bi-directional high-speed links from flange to SERDES mezzanine
- PGP PCI quad transceiver board
  - FPGA emulating the RCE and firmware from SLAC
  - We were not able to get it to take reliable data over the high-speed links (dropped packets, etc.)
- Used to verify that all 4 high-speed links could be established and send data between PC and cold FPGA
  - Data not validation quality



Validation Procedure

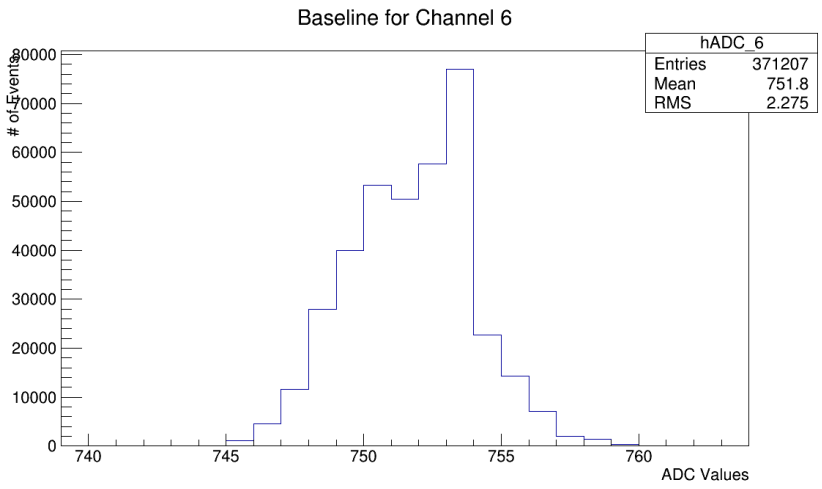
- Room temperature testing
  - Each FEMB was assembled on standoffs and visual inspection was done
  - Full test of functionality was done up through data recorded for noise and pulser settings
    - Several but usually not all FE ASIC gain and shaping settings
- 1 or 2 ASICs failed
  - Found to be pin solder problem
- Immediately after passing room temperature validation, FEMB cooled in styrofoam Dewar in LN2 over about 15 minutes
  - LV power supplies completely switched off
- LN2 testing
  - After several minutes in LN2, FEMB was powered on
  - All current draws carefully checked
  - Repeat of full functionality tests
  - Data taken for all FE and ADC ASIC settings
- 2 ADC ASICs and 17 FE ASICs failed in LN2 and were replaced
- After LN2 tests, board was uncabled and quickly bagged and allowed to warm up slowly
  - Rechecked for damage once warm

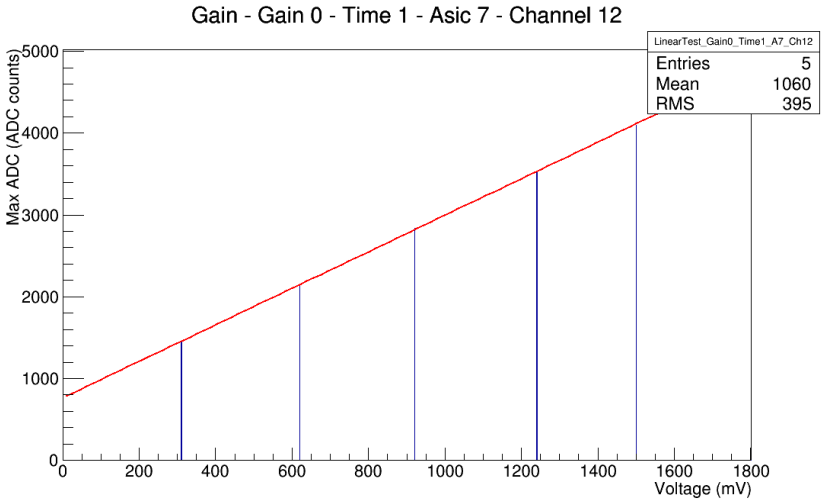
Outcome of Testing

- 16 validated FEMB were available for 35ton, but no spares
  - All FEMB functionality passed warm and LN2 tests
  - All FE and ADC ASICs functional in LN2 – few % bad channels
  - Data taken with compact DAQ for all FE and ADC ASIC settings for analysis
- Concerns that multiple LN2 cycles could damage FEMB
  - Once an FEMB passed all of the validation tests, it was not repeat cycled in LN2
- Small supply of FEMB, meant that we did not LN2 cycle one board repeatedly
  - Did not measure chance of FEMB failure on second cooldown

Test Data Analysis

All channels on all FEMB analyzed offline:
Distributions made of baseline, RMS noise, and linearity for both warm and LN2
Bad channels identified – most were already identified during the initial real-time board testing with the LabView GUI





35ton Test Summary

Date	20150827		
FEMB #	F25A9		
FPGA Board #	25		
Analog board #	9		
ASIC IDs			
Room Temperature Section			
		Result	
Tested Oscillator Installed	Y/N	Y	
Visual Inspection	Pass/Fail	Pass	
FEMB board power on at room temperature	Pass/Fail	Pass	
	5V current draw [A]		
	3.6V current draw [A]		
	2.8V current draw [A]		
	1.5V current draw [A]		
	2.1V current draw [A]		2.1V supply current draw dfrops to 0 occasionally, watch it
Quick functionality test at room temp	Pass/Fail		
-Boots from EEPROM	Y/N	Y	
-JTAG programming	Y/N	N	JTAG cable damaged!
-I2C interface	Y/N	N	Just doing ADC ASIC test
-ASIC SPI + sync	Y/N	Y	
-took noise + pulser data runs	Y/N	N	Just doing ADC ASIC test
Noise data run at room temp	Filename:	N	
Pulser data run at room temp	Filename:	N	
Cryogenic Section			
Boots from EEPROM (use I2C or link status)	Pass/Fail	Fail	EEPROM failed in LN2
FEMB board power on in liquid Nitrogen	Pass/Fail		

Log files for each FEMB test were kept in Google docs, entered by hand.
No suite of QC software or database was developed to automatically save records.

Analog Motherboards

- 35ton required 16 FEMBs, 4 per APA
- 19 total analog motherboards produced (one pre-production) and 18 tested
  - 16 analog motherboards passed final testing
- Ultimately one “bad” analog motherboard installed in 35ton
  - A8 had one FE ASIC that intermittently failed during power up in LN2
  - Was rushed to replace A11 when that board was damaged during installation

Analog #	Location	Status	Current Pairing	Action	Notes			
0	FNAL	OK	F20					PLAN as of Jun 18, 2015
1	FNAL	OK	F2					Debug A8
2	FNAL	OK	F22		ASIC 6 has lower than normal gain, borderline?			Debug A9
3	FNAL	OK	F3					Debug F9
4	FNAL	OK	F4					Test FPGA boards
5	FNAL	OK	F8		Large number of dead channels			
6	FNAL	OK	F6					
7	FNAL	OK	F5					Available FPGA board
8	FNAL	BAD	F24	DEBUG	ASIC 4 doesn't always work on power-on (DEBUG)			F4
9	BNL	BAD	F9	DEBUG	ASIC ? doesn't always work on power-on (DEBUG)			
10	FNAL	OK	F10					
11	BNL	BAD	F11		Damaged during APA installation			
12	FNAL	OK	F12					
13	FNAL	OK	F13					
14	FNAL	OK	F18					
15	FNAL	OK	F15					
16	FNAL	OK	F16					
17	FNAL	OK	F17					
18	INSTRUMENTAT	UNUSABLE	-					

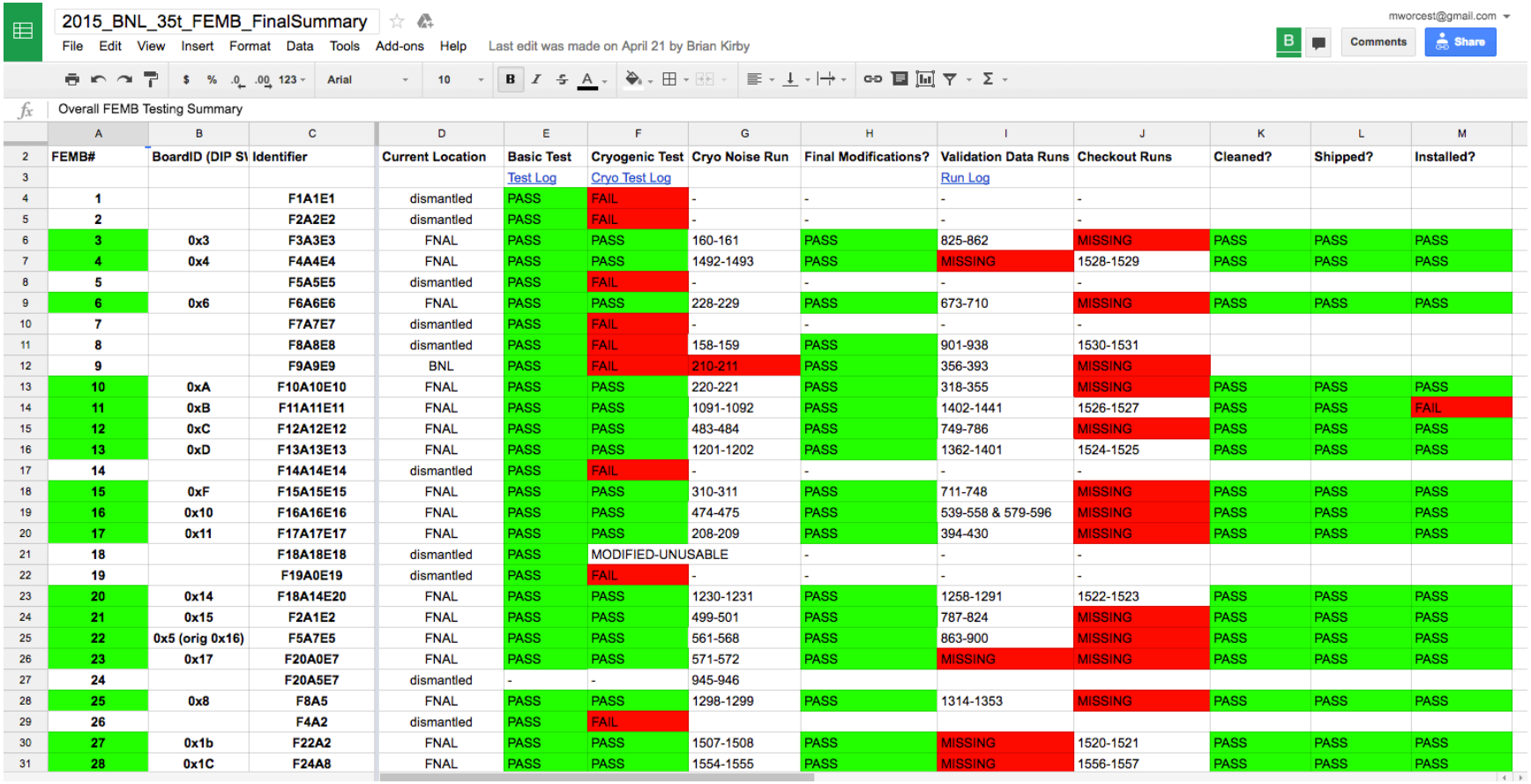
FPGA Mezzanines

- 35ton required 16 FEMBs, 4 per APA
- 19 total FPGA motherboards initially produced and tested
- 6 more assembled when 4 initial mezzanines failed to program the FPGA in LN2
  - 18 mezzanines passed final testing (2 spares)

FPGA #	Location	Status	Current Pairing	ACTION	Notes
1	BNL	BAD	-		JTAG FAILURE
2	FNAL	OK	A1		
3	FNAL	OK	A3		
4	FNAL	OK	A4		
5	FNAL	OK	A7		
6	FNAL	OK	A6		
7	BNL	BAD	-		JTAG FAILURE
8	FNAL	OK	A5		
9	BNL	BAD	A9		3.6V oscillation problem
10	FNAL	OK	A10		
11	FNAL	OK	A11		
12	FNAL	OK	A12		
13	FNAL	OK	A13		
14	BNL	BAD	-	RETEST	Streaming failure at room temperature
15	FNAL	OK	A15		
16	FNAL	OK	A16		
17	FNAL	OK	A17		
18	FNAL	OK	A14		Previously working, latest tests required large number of power cycles before boardd functioned correctly (see test notes)
19	Inst	BAD	-		JTAG FAILURE
20	FNAL	OK	A0		
Spare #1	BNL	BAD	-		JTAG FAILURE, note unlabeled
21	BNL	BAD	-		programming to and from EEPROM FAILED
22	FNAL	OK	A2		
23	BNL	OK	-		
24	FNAL	OK	A8		

Final Status Summary

Final status record for each analog+FPGA pair includes LN2 testing record, warm retesting, validation data location, data analysis, and installation status



2015_BNL_35t_FEMB_FinalSummary

File Edit View Insert Format Data Tools Add-ons Help Last edit was made on April 21 by Brian Kirby

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Comments Share

Arial 10

Overall FEMB Testing Summary

	A	B	C	D	E	F	G	H	I	J	K	L	M
2	FEMB#	BoardID (DIP S\	Identifier	Current Location	Basic Test	Cryogenic Test	Cryo Noise Run	Final Modifications?	Validation Data Runs	Checkout Runs	Cleaned?	Shipped?	Installed?
3					Test Log	Cryo Test Log			Run Log				
4	1		F1A1E1	dismantled	PASS	FAIL	-	-	-	-			
5	2		F2A2E2	dismantled	PASS	FAIL	-	-	-	-			
6	3	0x3	F3A3E3	FNAL	PASS	PASS	160-161	PASS	825-862	MISSING	PASS	PASS	PASS
7	4	0x4	F4A4E4	FNAL	PASS	PASS	1492-1493	PASS	MISSING	1528-1529	PASS	PASS	PASS
8	5		F5A5E5	dismantled	PASS	FAIL	-	-	-	-			
9	6	0x6	F6A6E6	FNAL	PASS	PASS	228-229	PASS	673-710	MISSING	PASS	PASS	PASS
10	7		F7A7E7	dismantled	PASS	FAIL	-	-	-	-			
11	8		F8A8E8	dismantled	PASS	FAIL	158-159	PASS	901-938	1530-1531			
12	9		F9A9E9	BNL	PASS	FAIL	210-211	PASS	356-393	MISSING			
13	10	0xA	F10A10E10	FNAL	PASS	PASS	220-221	PASS	318-355	MISSING	PASS	PASS	PASS
14	11	0xB	F11A11E11	FNAL	PASS	PASS	1091-1092	PASS	1402-1441	1526-1527	PASS	PASS	FAIL
15	12	0xC	F12A12E12	FNAL	PASS	PASS	483-484	PASS	749-786	MISSING	PASS	PASS	PASS
16	13	0xD	F13A13E13	FNAL	PASS	PASS	1201-1202	PASS	1362-1401	1524-1525	PASS	PASS	PASS
17	14		F14A14E14	dismantled	PASS	FAIL	-	-	-	-			
18	15	0xF	F15A15E15	FNAL	PASS	PASS	310-311	PASS	711-748	MISSING	PASS	PASS	PASS
19	16	0x10	F16A16E16	FNAL	PASS	PASS	474-475	PASS	539-558 & 579-596	MISSING	PASS	PASS	PASS
20	17	0x11	F17A17E17	FNAL	PASS	PASS	208-209	PASS	394-430	MISSING	PASS	PASS	PASS
21	18		F18A18E18	dismantled	PASS	MODIFIED-UNUSABLE		-	-	-			
22	19		F19A0E19	dismantled	PASS	FAIL	-	-	-	-			
23	20	0x14	F18A14E20	FNAL	PASS	PASS	1230-1231	PASS	1258-1291	1522-1523	PASS	PASS	PASS
24	21	0x15	F2A1E2	FNAL	PASS	PASS	499-501	PASS	787-824	MISSING	PASS	PASS	PASS
25	22	0x5 (orig 0x16)	F5A7E5	FNAL	PASS	PASS	561-568	PASS	863-900	MISSING	PASS	PASS	PASS
26	23	0x17	F20A0E7	FNAL	PASS	PASS	571-572	PASS	MISSING	MISSING	PASS	PASS	PASS
27	24		F20A5E7	dismantled	-	-	945-946						
28	25	0x8	F8A5	FNAL	PASS	PASS	1298-1299	PASS	1314-1353	MISSING	PASS	PASS	PASS
29	26		F4A2	dismantled	PASS	FAIL							
30	27	0x1b	F22A2	FNAL	PASS	PASS	1507-1508	PASS	MISSING	1520-1521	PASS	PASS	PASS
31	28	0x1C	F24A8	FNAL	PASS	PASS	1554-1555	PASS	MISSING	1556-1557	PASS	PASS	PASS

Lessons Learned

- Manpower was low
  - No full-time physicist was committed to lead effort
  - Slowed ramp up and testing effort
- Time was very short
  - Electronics were already behind schedule when production boards were ready for testing
  - Physicists not have time to study FEMB performance in detail
  - Focus of physicist testing was to get 16 operational FEMB to Fermilab as quickly as possible
    - Single bad channels not cataloged and studied
    - Noise tests with wire capacitance and careful shielding and grounding were not implemented
    - Most common problems (FPGA programming over JTAG failure, bad ASICs in LN2) were not studied, parts/ASICs were simply replaced
  - Result was FEMB installed without detailed understanding by physicists
    - Did not prepare 35ton for noise issues found in the detector

Lessons Learned

- QA/QC plan not sufficient
  - Did not develop an automatic testing procedure and database
    - Finding problems and keeping records during testing relied on careful attention from testers, some records were found to be incomplete
    - Could usually reconstruct what happened with later data analysis…
    - But one FEMB with known bad ASICs was delivered to Fermilab and had to be returned to BNL for replacement
  - LabView DAQ was cumbersome
    - Required lots of button pushing to change FE and ADC ASIC settings and program SPI
    - Easy to make mistakes and get settings wrong
    - These errors were usually found in data analysis later
  - No tests with multiple FEMB on actual APA or mechanical mockup was done
    - Did not prepare 35ton for warping under mechanical stress in LAr
- Communication to 35ton collaboration was ineffective
  - Updates were given to the LBNE cold electronics group
    - Attendance from both design experts and 35ton leadership at these meetings was low
  - Physicists testing should have done a better job of regular reporting to a wider audience
  - Result was 35ton leadership had some nasty surprises (i.e. stuck ADC codes)

Conclusions

- 16 fully validated FEMB were available for 35ton, but no spares
- Critical effort from BNL Instrumentation to produce the FEMB
- From the point of view of the physicists, important lessons learned regarding:
  - Time required to produce and test cold electronics
  - Developing and implementing QA/QC plan
  - Communicating to design experts and collaboration